EN - For pricing and availability in your local country please visit one of the below links:

DE - Informationen zu Preisen und Verfügbarkeit in Ihrem Land erhalten Sie über die unten aufgeführten Links:

FR - Pour connaître les tarifs et la disponibilité dans votre pays, cliquez sur l'un des liens suivants:

TPA3130D2EVM

EN
This Datasheet is presented by the manufacturer

DE
Dieses Datenblatt wird vom Hersteller bereitgestellt

FR
Cette fiche technique est présentée par le fabricant

50W Filter-Free Class-D Stereo Amplifier with AM Avoidance

Check for Samples: TPA3116D2

FEATURES

- **Supports Multiple Output Configurations**
  - **2×50-W into a 4-Ω BTL Load at 21 V**
  - **2×25-W into a 4-Ω BTL Load at 14.4 V**
- **Wide Voltage Range: 6 V – 26 V**
- **Automotive Load-Dump Compliant**
- **Efficient Class-D Operation**
  - **>90% Power Efficiency Combined with Low Idle Loss Greatly Reduces Heat Sink Size**
- **Feedback Power Stage Architecture**
  - **Improved PSRR Reduces Power Supply Performance Requirements**
  - **High Damping Factor Provides for Tighter, More Accurate Sound with Improved Bass Response**
- **Differential Inputs**
- **Multiple Switching Frequencies**
  - **AM Avoidance**
  - **Frequency Synchronization**
- **Power Limit**
- **Stereo and Mono Mode**
  - **Single Filter Mono Mode**
- **Single Power Supply**
- **Integrated Self-Protection Circuits Including Over-Voltage, Under-Voltage, Over-Temperature, DC-Detect, and Short Circuit with Error Reporting**
- **Thermally Enhanced Packages**
  - **DAD (32-pin HTSSOP Pad-up)**
- **–40°C to +85°C Ambient Temperature Range**

APPLICATIONS

- **Mini-Micro Component, Speaker Bar, Docks**
- **After-Market Automotive**
- **CRT TV**
- **Consumer Audio Applications**

PRODUCT PREVIEW

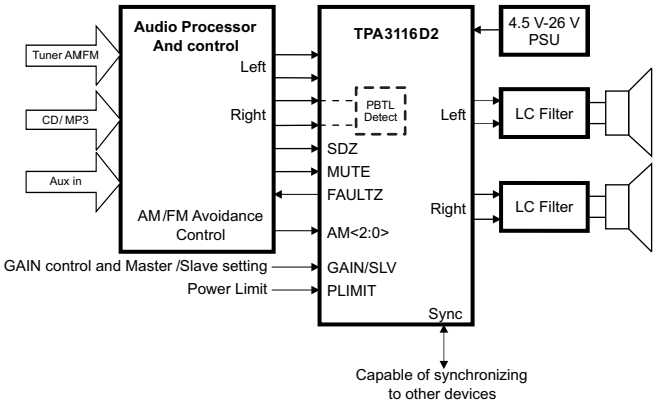
DESCRIPTION

The TPA3116D2 is a stereo 50-W efficient, stereo digital amplifier power stage for driving 2 bridge-tied speakers or up to 100 W single parallel bridge-tied load. The TPA3116D2 can drive a speaker with an impedance as low as 3.2 Ω (4 Ω typical). The high efficiency of the TPA3116D2 allows for a small external heat sink in the 32p DAD package and can even run without a heat sink for music power.

The TPA3116D2 employs a multiple switching frequency option to avoid AM interference.

The TPA3116D2 is fully protected against faults with short-circuit protection and thermal protection as well as over-voltage, under-voltage, and DC protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

SIMPLIFIED APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

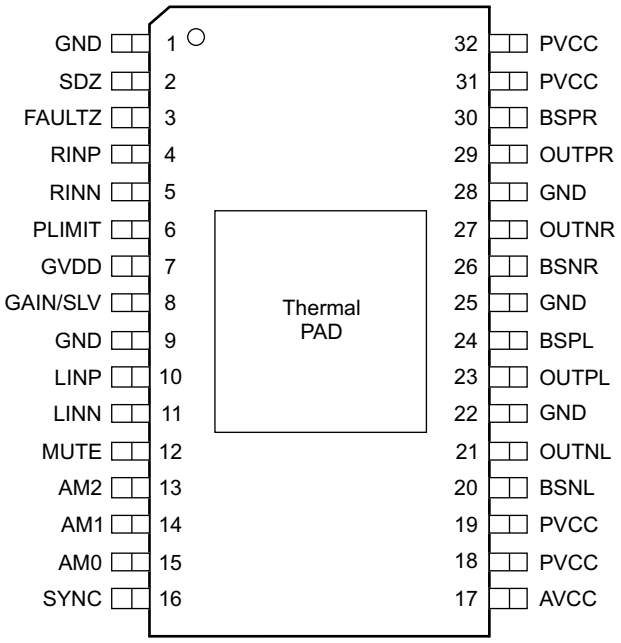
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL ASSIGNMENT

The TPA3116D2 is available in the thermally enhanced package:

32-PIN HTSSOP PACKAGE (DAD)

PACKAGE
(TOP VIEW)



Terminal Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	I	Connect to GND
2	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO	General fault reporting including Over-current_PVCC, OVP_DVDD FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	RINP	I	Positive audio input for right channel. Biased at 3 V.
5	RINN	I	Negative audio input for right channel. Biased at 3 V.
6	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor.
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9	GND	G	Power Ground
10	LINP	I	Negative audio input for left channel. Biased at 3 V.
11	LINN	I	Positive audio input for left channel. Biased at 3 V.
12	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs OFF, LOW = outputs ON). TTL logic levels with compliance to AVCC.
13	AM2	I	AM Avoidance Frequency Selection

(1) **TYPE**: DO = Digital Output, I = Analog Input, G = General Ground, PBY = Power Bypass, PO = Power Output, PI = Power Input, BST = Boot Strap.

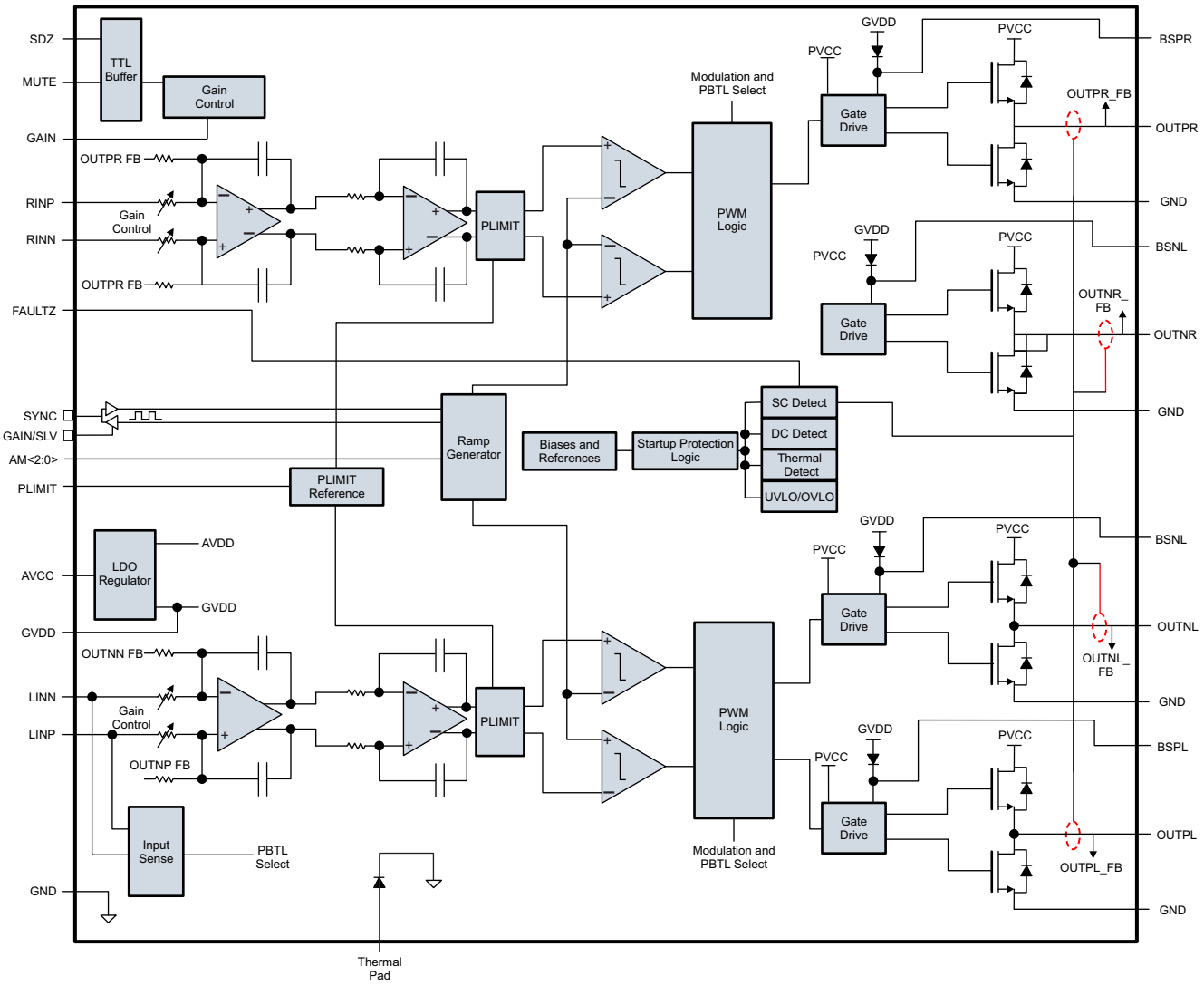
PRODUCT PREVIEW

Terminal Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
14	AM1	I	AM Avoidance Frequency Selection
15	AM0	I	AM Avoidance Frequency Selection
16	SYNC	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal. Input signal not to exceed GVDD (7 V).
17	AVCC	P	Analog Supply
18	PVCC	P	Power supply
19	PVCC	P	Power supply
20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X7R ceramic cap to OUTPL
21	OUTNL	PO	Negative left channel output
22	GND	G	Ground
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X7R ceramic cap to OUTNL
25	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X7R ceramic cap to OUTNR
27	OUTNR	PO	Negative right channel output
28	GND	G	Ground
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X7R ceramic cap to OUTPR
31	PVCC	PI	Power supply
32	PVCC	PI	Power supply
33	Thermal Pad or PowerPAD	G	Connect to GND for best system performance. If not connected to GND, leave floating.

PRODUCT PREVIEW

SYSTEM BLOCK DIAGRAM



PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage, V_{CC}	PVCC, AVCC	–0.3 to 30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3 to 6.3	V
	PLIMIT, GAIN / SLV, SYNC	–0.3 to GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ	–0.3 to PVCC+0.3	V
Operating free-air temperature, T_A		–40 to 85	°C
Operating junction temperature range, T_J		–40 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C
Electrostatic discharge: Human body model, ESD		±2	kV
Electrostatic discharge: Charged device model, ESD		±500	V

THERMAL INFORMATION

THERMAL METRIC(1)		TPA3116D2		UNITS
		DAD (no heatsink)	DAD (with heatsink)	
		32 PINS	32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance			°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance			
θ_{JB}	Junction-to-board thermal resistance			
ψ_{JT}	Junction-to-top characterization parameter			
ψ_{JB}	Junction-to-board characterization parameter			
θ_{JCbot}	Junction-to-case (bottom) thermal resistance			

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	6		26	V
		PVCC, AVCC	6		20	
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PVCC = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ (V_I = 2 V, VCC = 18 V)			50	μA
T_A	Operating free-air temperature		–40		85	°C
R_L(BTL)	Load Impedance	Output filter: L = 10 μH, C = 680 nF	3.2	4		Ω
R_L(PBTL)		Output filter: L = 10 μH, C = 1 μF	1.6	2		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			μH

PRODUCT PREVIEW

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	VI = 0 V, Gain = 36 dB		1.5	15	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, no load, PVCC = 12 V		20	35	mA
		SDZ = 2 V, no load, PVCC = 24 V		32	50	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, no load, PVCC = 12 V		200		µA
		SDZ = 0.8 V, no load, PVCC = 24 V		250	400	
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	VCC = 21 V, I_{out} = 500 mA, T_J = 25°C		120		mΩ
G	Gain (BTL)	R1 = open, R2 = 5.6 Ω	19	20	21	dB
		R1 = 100 kΩ, R2 = 20 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 75 kΩ, R2 = 47 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 47 kΩ, R2 = 75 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 16 kΩ, R2 = 100 kΩ	35	36	37	
t_{on}	Turn-on time	SDZ = 2 V		10		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V		2		µs
GVDD	Gate Drive Supply	IGVDD < 200 µA	6.4	6.9	7.4	V
V_O	Output Voltage maximum under PLIMIT control	V(PLIMIT) = 2 V; V_I = 1 Vrms	6.75	7.90	8.75	V

PRODUCT PREVIEW

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power Supply ripple rejection	200 mVPP ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to AGND		–70		dB
PO	Continuous output power	THD+N = 10%, f = 1 kHz, VCC = 12 V		20		W
		THD+N = 10%, f = 1 kHz, VCC = 21 V		50		
THD+N	Total harmonic distortion + noise	VCC = 21 V, f = 1 kHz, PO = 25 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		μV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	AM2=0, AM1=0, AM0=0	376	400	424	kHz
		AM2=0, AM1=0, AM0=1	470	500	530	
		AM2=0, AM1=1, AM0=0	564	600	636	
		AM2=0, AM1=1, AM0=1	Reserved			
		AM2=1, AM1=0, AM0=0				
		AM2=1, AM1=0, AM0=1				
		AM2=1, AM1=1, AM0=0				
		AM2=1, AM1=1, AM0=1				
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION +NOISE (BTL) vs FREQUENCY

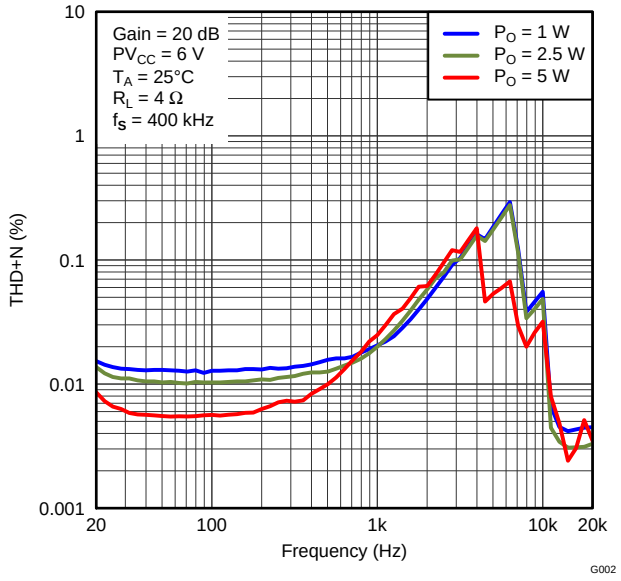


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

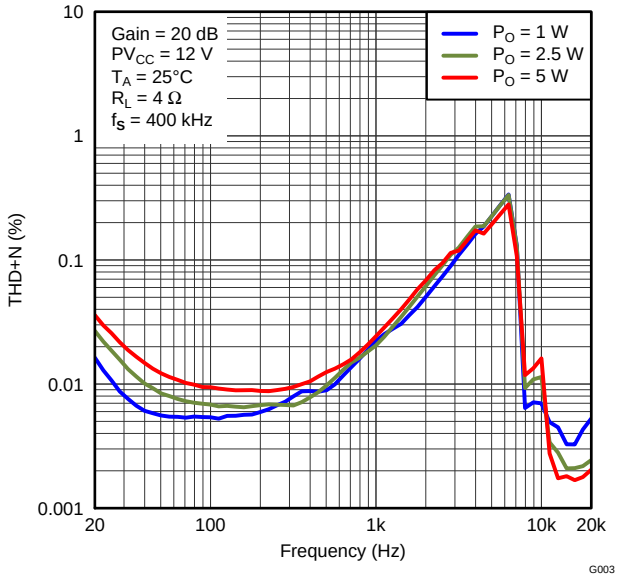


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

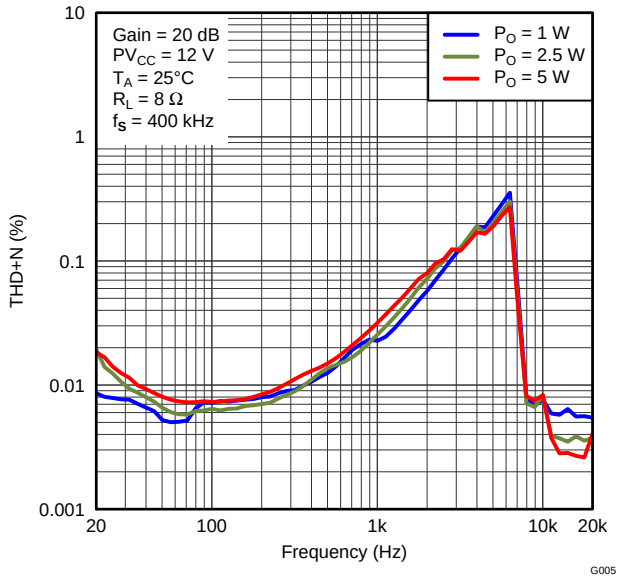


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY

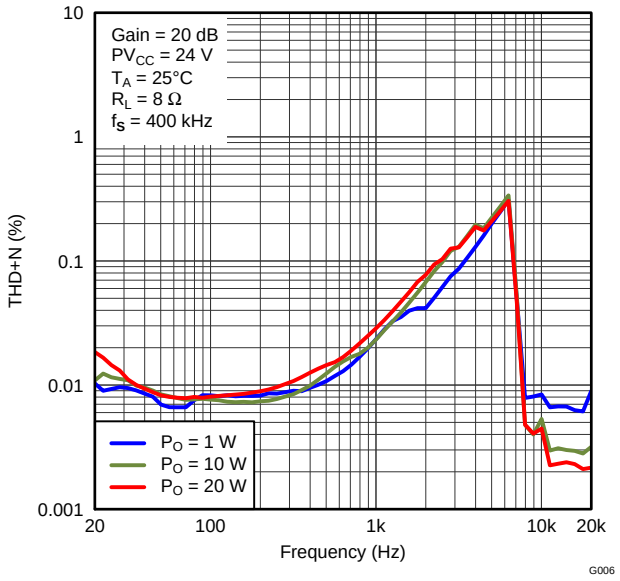


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

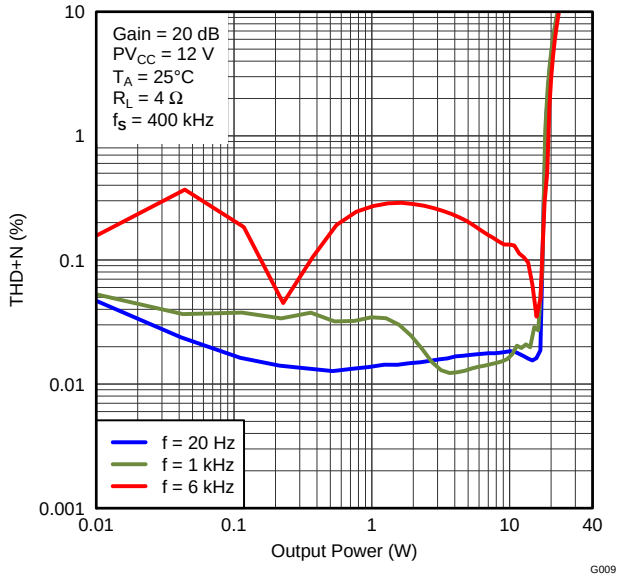


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

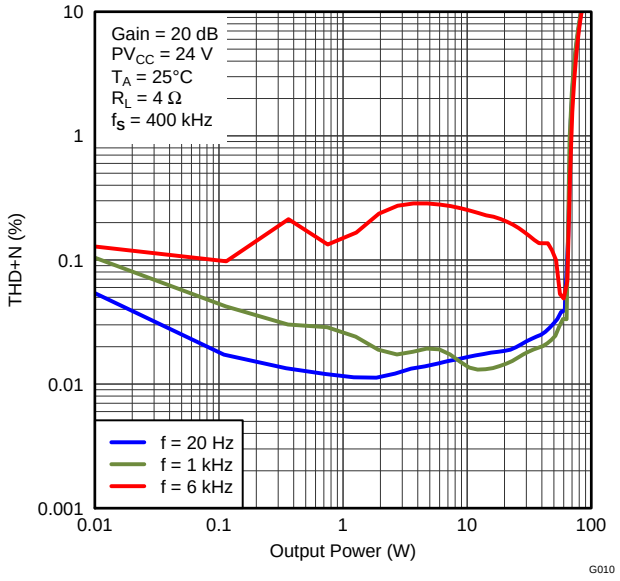


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

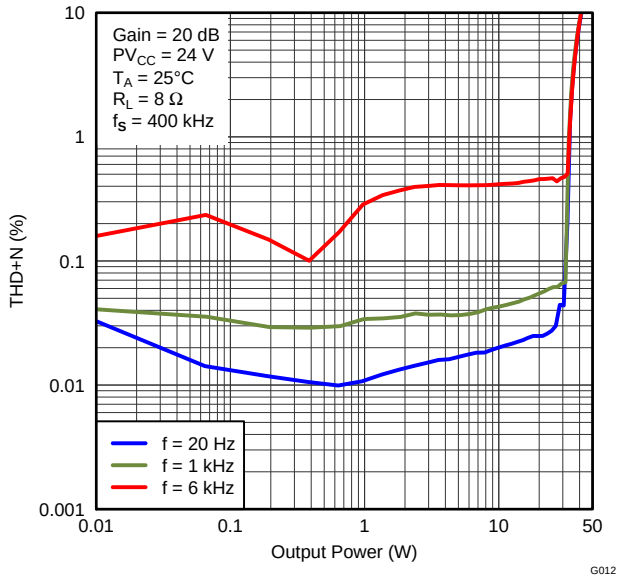


Figure 7.

GAIN/PHASE (BTL) vs FREQUENCY

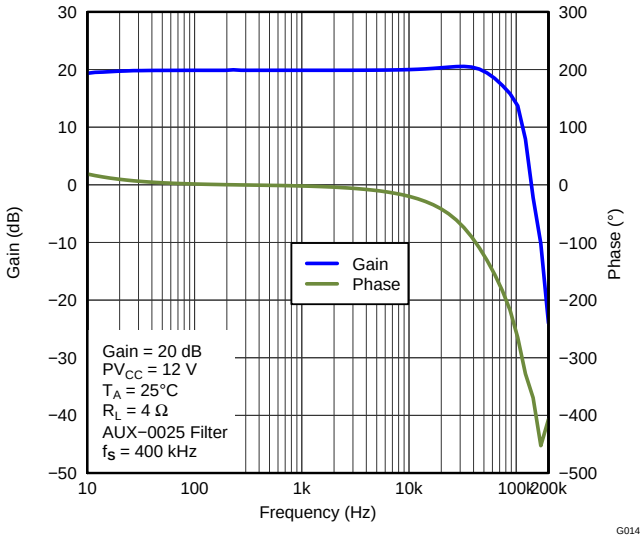


Figure 8.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT POWER (BTL) vs SUPPLY VOLTAGE

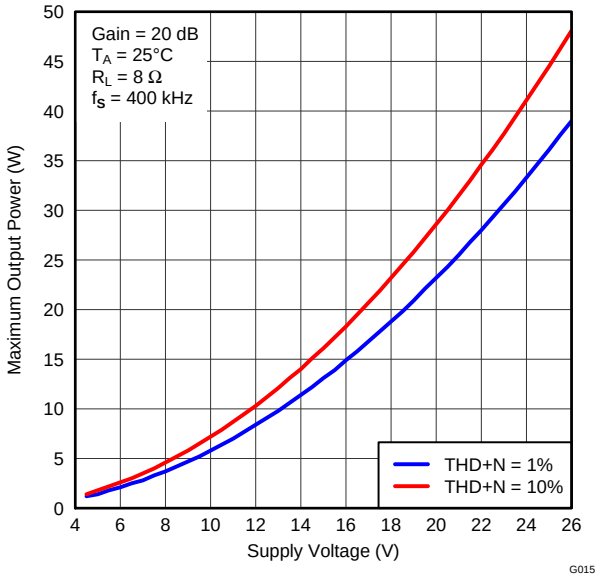


Figure 9.

MAXIMUM OUTPUT POWER (BTL) vs SUPPLY VOLTAGE

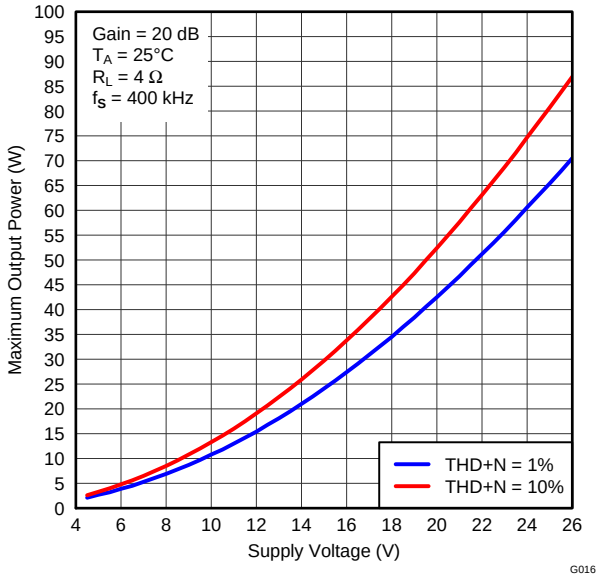


Figure 10.

OUTPUT CURRENT (BTL) vs TOTAL OUTPUT POWER

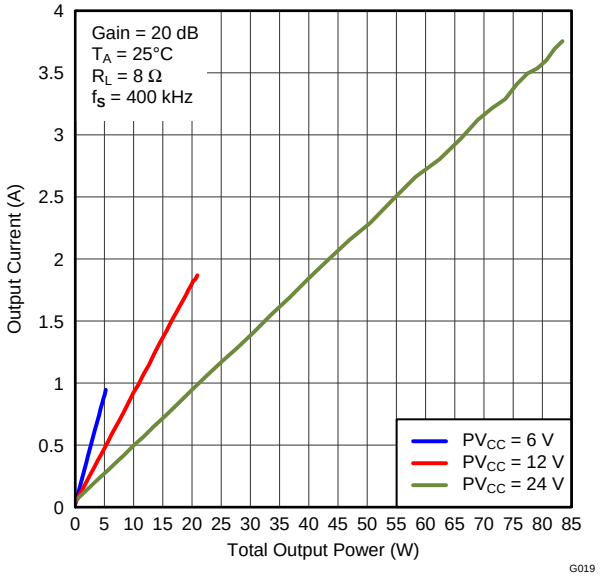


Figure 11.

CROSSTALK (BTL) vs FREQUENCY

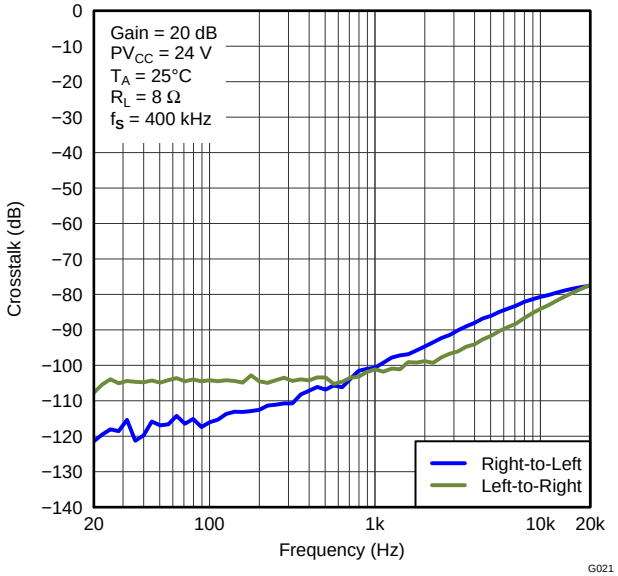


Figure 12.

TYPICAL CHARACTERISTICS (continued)

SUPPLY RIPPLE REJECTION RATIO (BTL) vs FREQUENCY

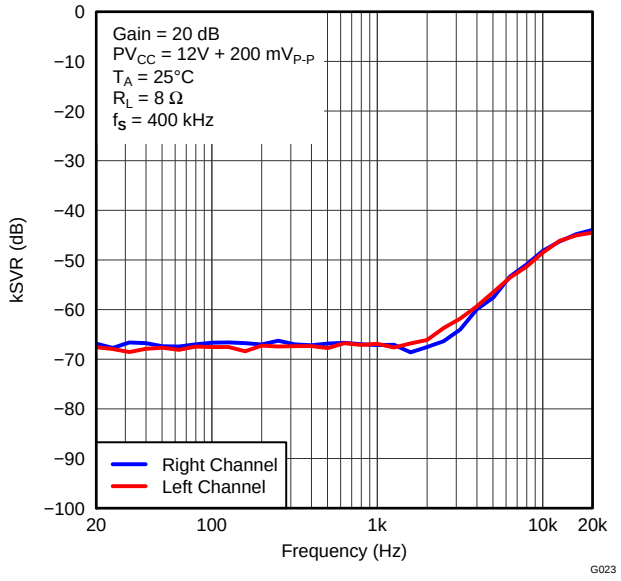


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE (PBTL) vs FREQUENCY

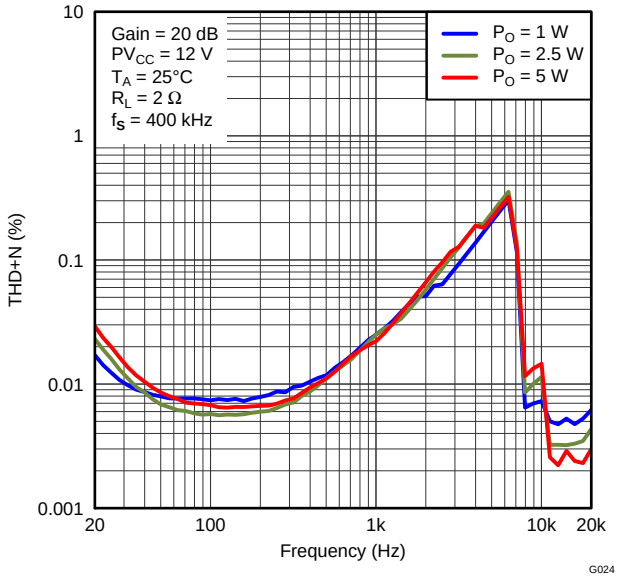


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE (PBTL) vs OUTPUT POWER

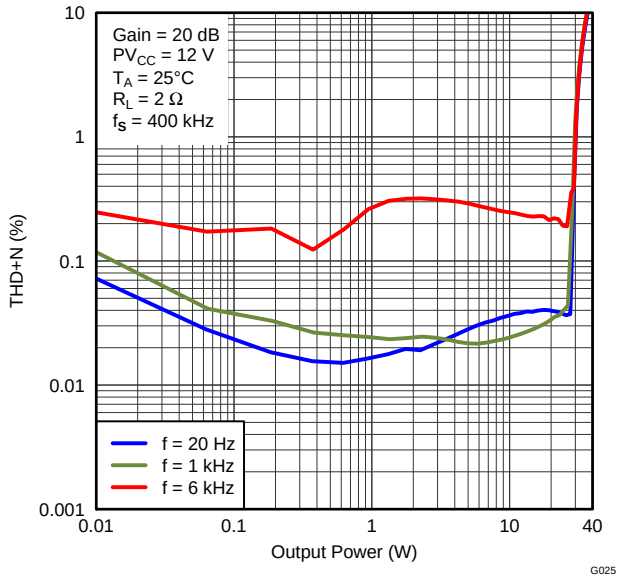


Figure 15.

MAXIMUM OUTPUT POWER (PBTL) vs SUPPLY VOLTAGE

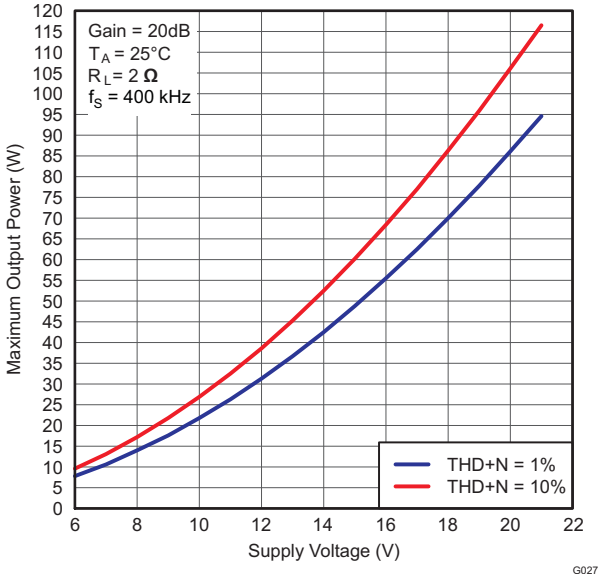


Figure 16.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

POWER EFFICIENCY (PBTL)
vs
OUTPUT POWER

Figure 17.

TOTAL HARMONIC DISTORTION + NOISE (PBTL)
vs
FREQUENCY

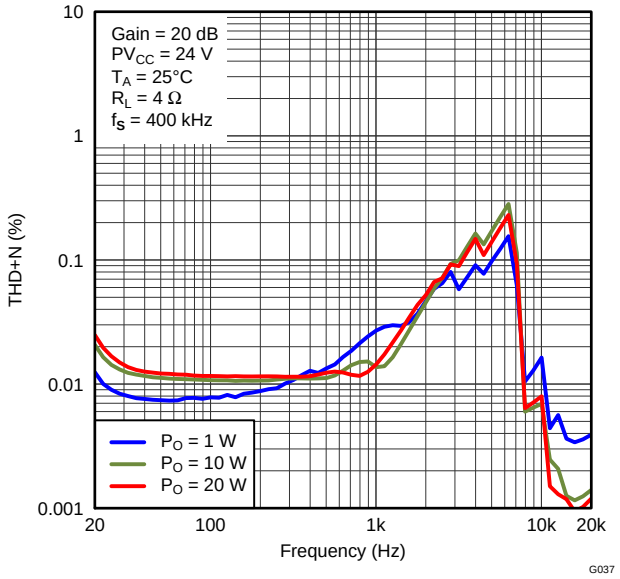


Figure 18.

TOTAL HARMONIC DISTORTION + NOISE (PBTL)
vs
OUTPUT POWER

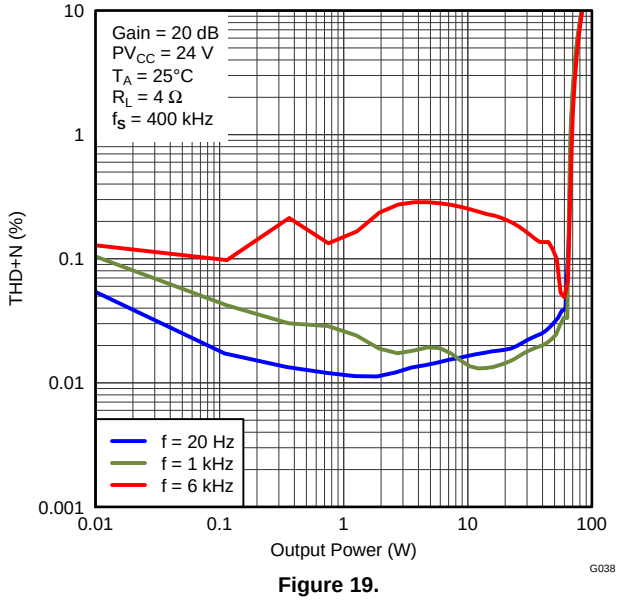


Figure 19.

DEVICE INFORMATION

TYPICAL APPLICATION

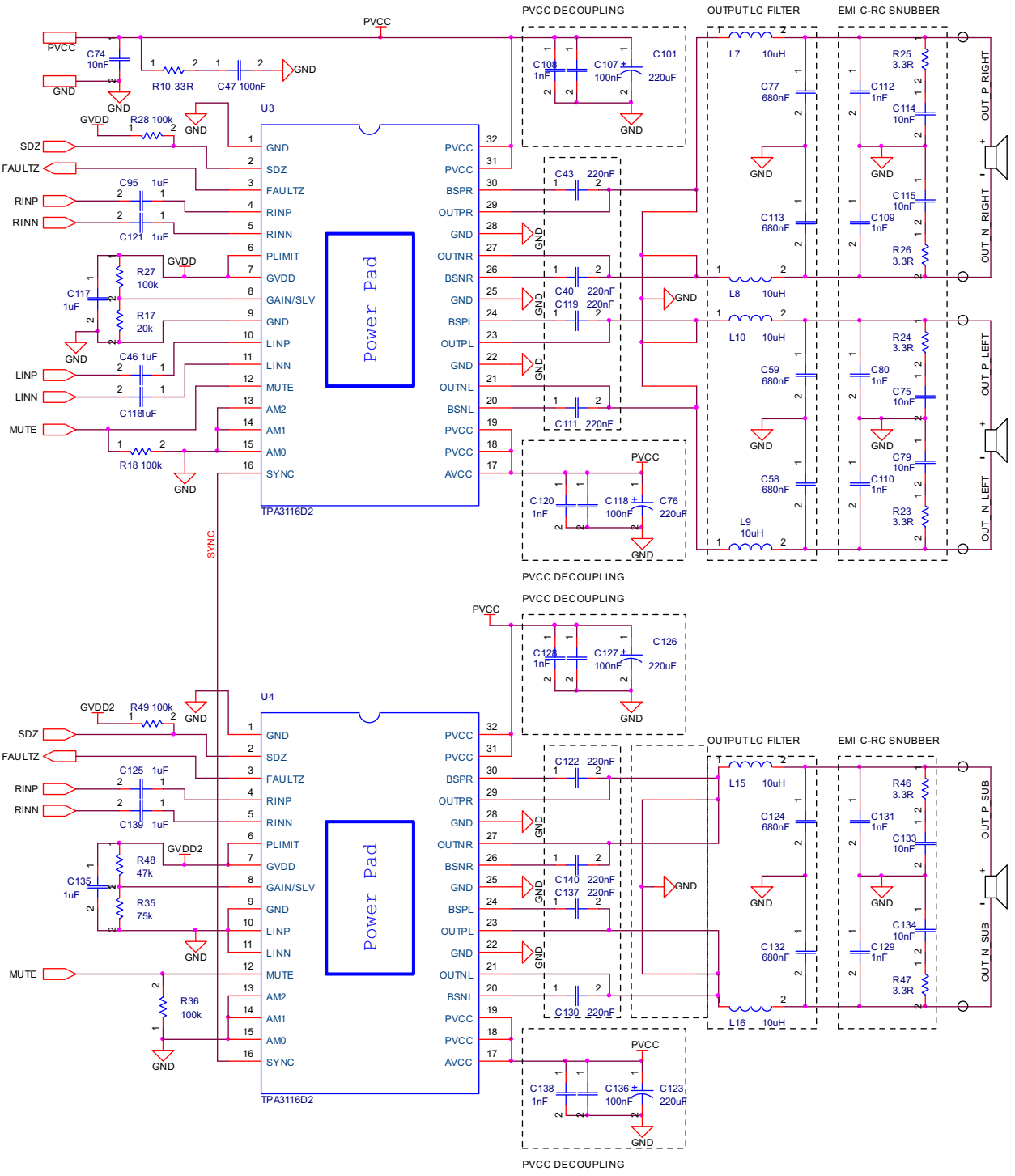


Figure 20. Schematic

A 2.1 solution, U3 TPA3116D2 in Master, BTL, gain of 20 dB. Power limit not implemented. U4 in Slave, PBTL gain if 20dB. A 10 µH – 680 nF second order output filter is used for all outputs. Inputs are connected for differential input.

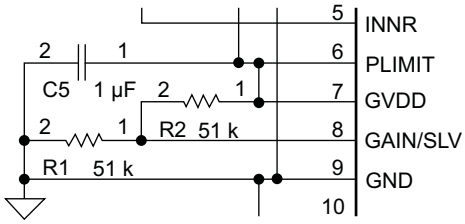
PRODUCT PREVIEW

GAIN SETTING AND MASTER / SLAVE

The gain of the TPA3116D2 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 shows the recommended resistor values and the state and gain:

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)	R2 (to GVDD)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ



In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

INPUT IMPEDANCE

The TPA3116D2 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. Table 1 lists the values from min to max gain The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs need to be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

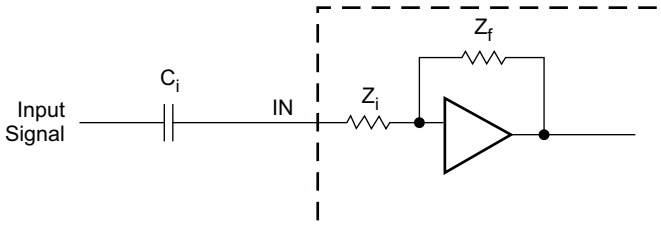
$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 2 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1 µF can be used.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

PRODUCT PREVIEW



The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum or ceramic. If a polarized type is used the positive connection should face the input pins of TPA3116D2 are biased to 3 Vdc.

START-UP/SHUTDOWN OPERATION

The TPA3116D2 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle.

PLIMIT OPERATION

The TPA3116D2 has a build-in voltage limited that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1 µF capacitor from pin PLIMIT to ground to ensure stability.

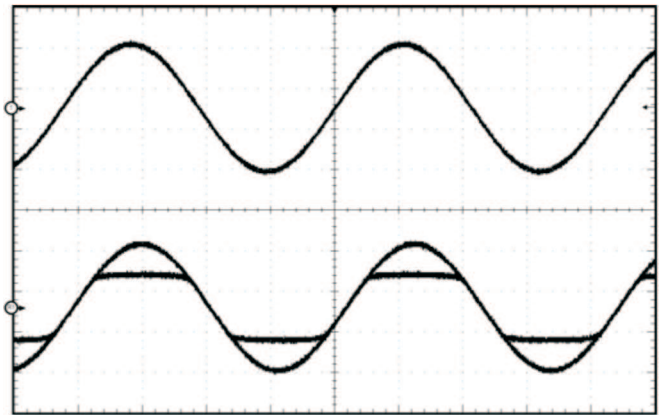


Figure 21. POWER LIMIT Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is approximately 4 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

PRODUCT PREVIEW

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \text{ for unclipped power} \quad (2)$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 3. POWER LIMIT Example

SUPPLY VOLTAGE	GAIN	PLIMIT VOLTAGE	R3 (to GND)	R4 (to GVDD)	OUTPUT POWER	OUTPUT VOLTAGE (V_{p-p})
24 V	26 dB	2.94	39 kΩ	51 kΩ	15	25.2
24 V	26 dB	2.34	39 kΩ	75 kΩ	10	20
24 V	26 dB	1.62	24 kΩ	75 kΩ	5	14
24 V	26 dB	6.97	Open	Short	12.1	27.7
24 V	20 dB	3.00	43 kΩ	56 kΩ	10	23
12 V	20 dB	1.86	30 kΩ	82 kΩ	5	14.8
12 V	20 dB	6.97	Open	Short	10.6	23.5
12 V	20 dB	1.76	27 kΩ	82 kΩ	5	15

PRODUCT PREVIEW

GVDD SUPPLY

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X7R ceramic 1 µF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

BSPx AND BSNx CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220 nF ceramic capacitor, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in fig xx) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL INPUTS

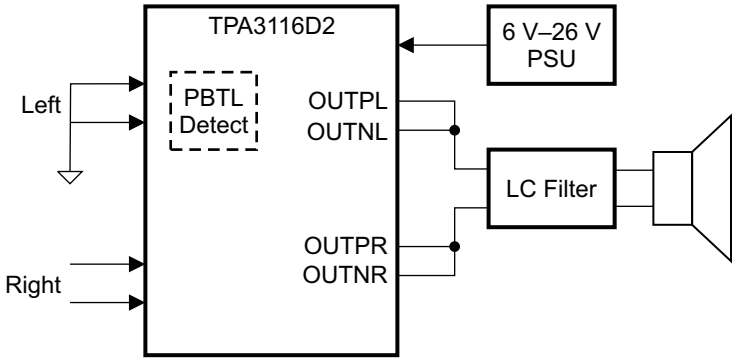
The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3116D2 with a differential source, connect the positive lead of the audio source to the INPx input and the negative lead from the audio source to the INNx input. To use the TPA3116D2 with a single-ended source, ac ground the INPx or INNx input through a capacitor equal in value to the input capacitor on INNx or INPx and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 10 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

MONO MODE (PBTL)

The TPA3116D2 can be connected in MONO mode enabling up to 100W output power. This is done by:

- Connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative terminal
- Analog input signal is applied to INPR and INNR



DEVICE PROTECTION SYSTEM

The TPA3116D2 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to the fault table below:

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

The TPA3116D2 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

THERMAL PROTECTION

Thermal protection on the TPA3116D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the FAULTZ terminal.

TPA3116D2 MODULATION SCHEME

The TPA3116D2 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

PRODUCT PREVIEW

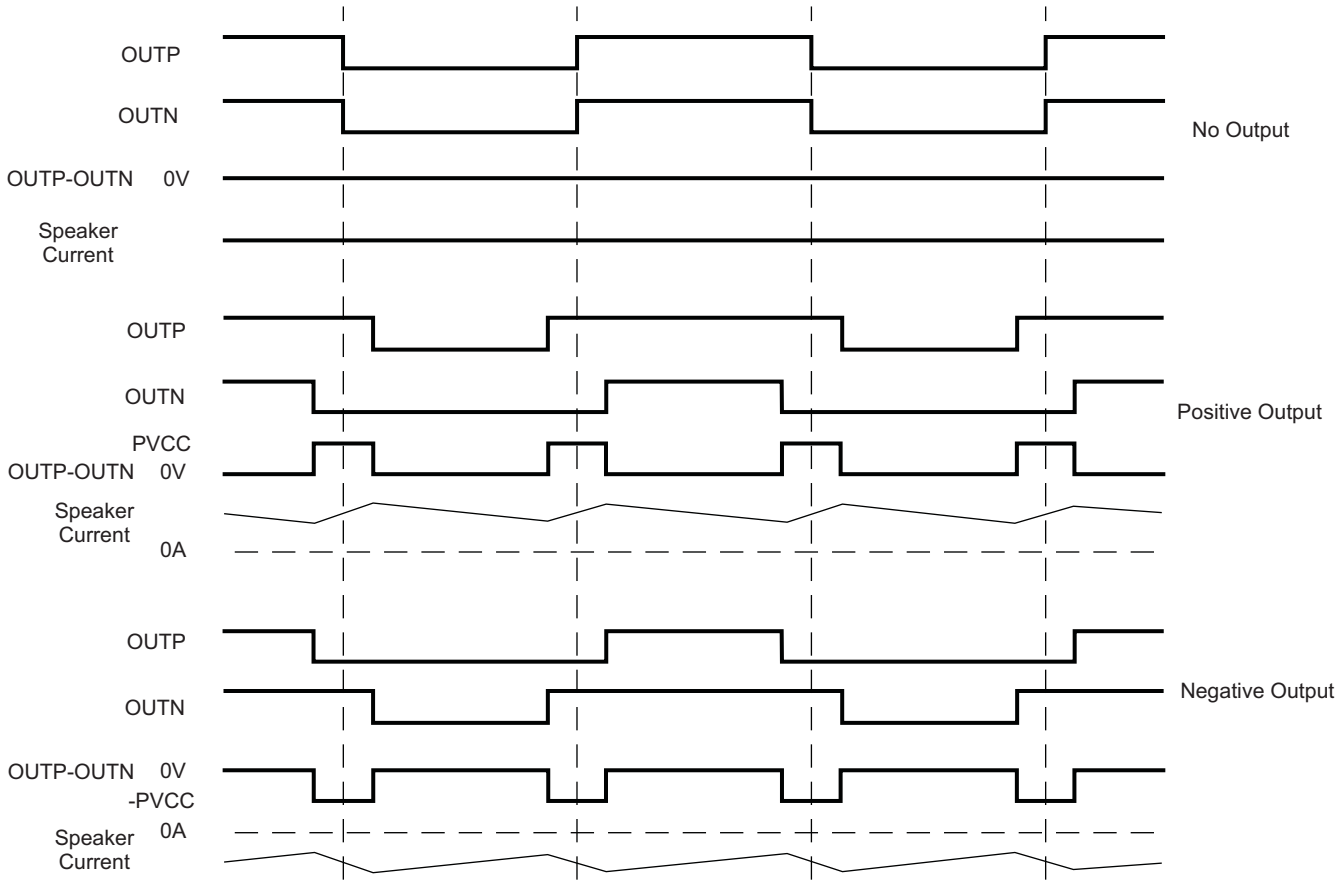


Figure 22. BD Mode Modulation

EFFICIENCY: LC FILTER REQUIRED WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3116D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

FERRITE BEAD FILTER CONSIDERATIONS

Using the Advanced Emissions Suppression Technology in the TPA3116D2 amplifier it is possible to design a high efficiency class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz

range which is key to the operation of the class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3116D2 include xxxx and yyy from kkkk and the zzzz from mmmmm.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

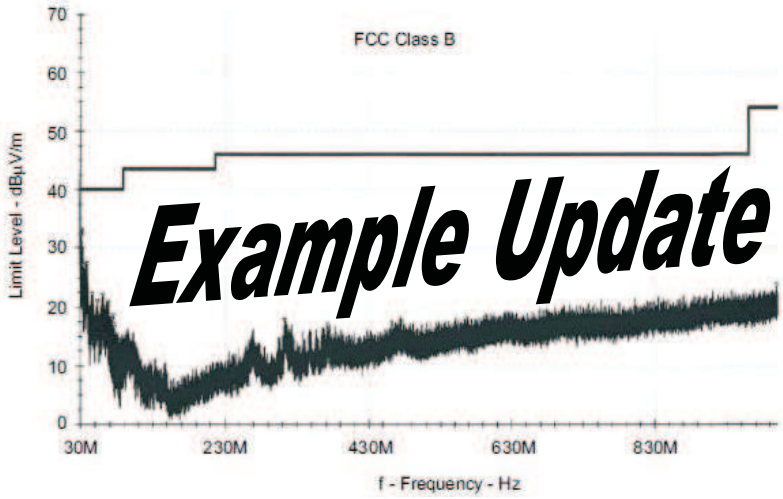


Figure 23.

WHEN TO USE AN OUTPUT FILTER FOR EMI SUPPRESSION

The TPA3116D2 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3116D2 EVM passes FCC class-B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

PRODUCT PREVIEW

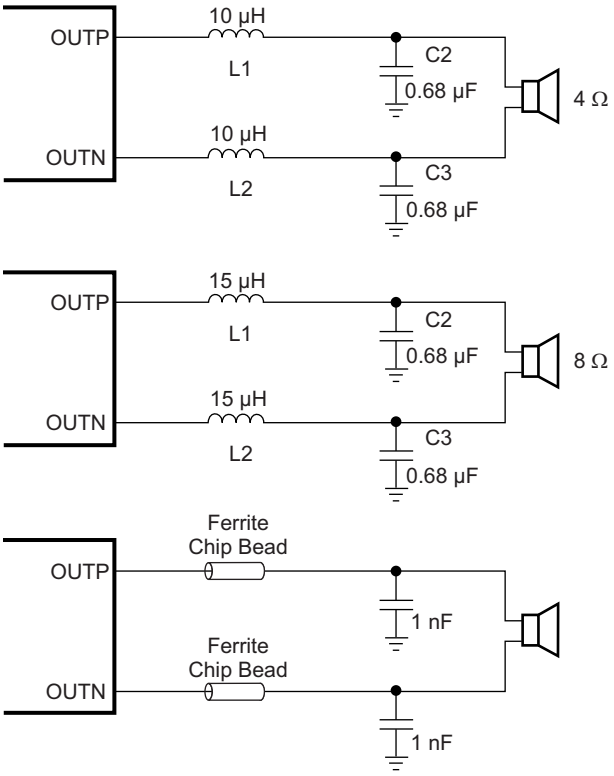


Figure 24.

AM AVOIDANCE EMI REDUCTION

To reduce interference in the AM radio band, the TPA3116D2 has the ability to change the switching frequency via AM<2:0> pins. The recommended frequencies are listed in Table 4. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

Table 4. AM Frequencies

US					EUROPEAN				
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
					522-540	400	0	0	0
540-917	500	0	0	1	540-914	500	0	0	1
917-1125	600 (or 400)	0 0	1 0	0 0	914-1122	600 (or 400)	0 0	1 0	0 0
1125-1375	500	0	0	1	1122-1373	500	0	0	1
1375-1547	600 (or 400)	0 0	1 0	0 0	1373-1548	600 (or 400)	0 0	1 0	0 0
1547-1700	600 (or 500)	0 0	1 0	0 1	1548-1701	600 (or 500)	0 0	1 0	0 1

PRINTED-CIRCUIT BOARD (PCB LAYOUT)

The TPA3116D2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

PRODUCT PREVIEW

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (2200 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3116D2 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA3116D2.
- Output filter — The ferrite EMI filter (see Figure 24) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

For an example layout, see the TPA3116D2 Evaluation Module (TPA3116D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

HEATSINK USED ON THE EVM

The heat sink used on the EVM is an 14x25x50 mm extruded aluminum heat sink with tree fins: see drawing below:

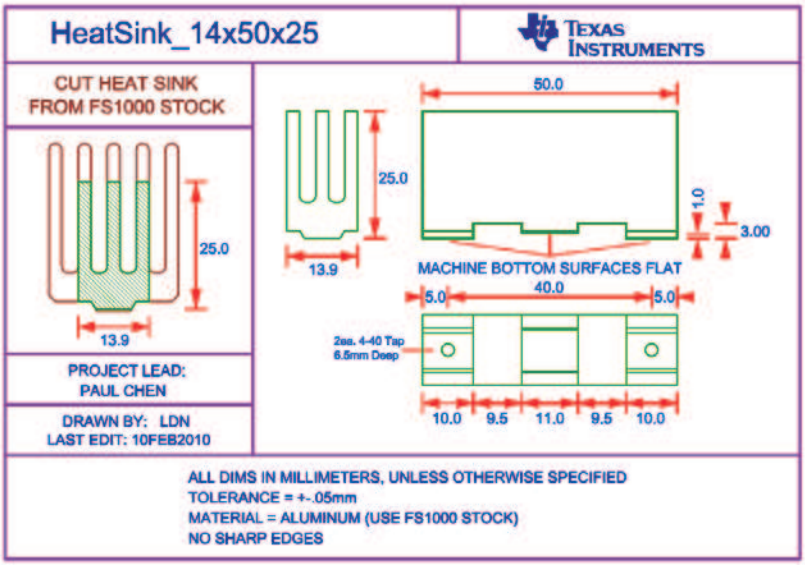


Figure 25.

This size heat sink have shown to be sufficient for continues output power. The crest factor of music and having airflow will lower the requirement for the heat sink size and smaller types can be used.

FOOTPRINT COMPATIBLE DEVICE FAMILY

TPA3116D2

TPA3118D2

TPA3130D2

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA3116D2DAD	ACTIVE	HTSSOP	DAD	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3116 D2	Samples
TPA3116D2DADR	ACTIVE	HTSSOP	DAD	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3116 D2	Samples
TPA3118D2DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3118	Samples
TPA3118D2DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3118	Samples
TPA3130D2DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3130	Samples
TPA3130D2DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3130	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

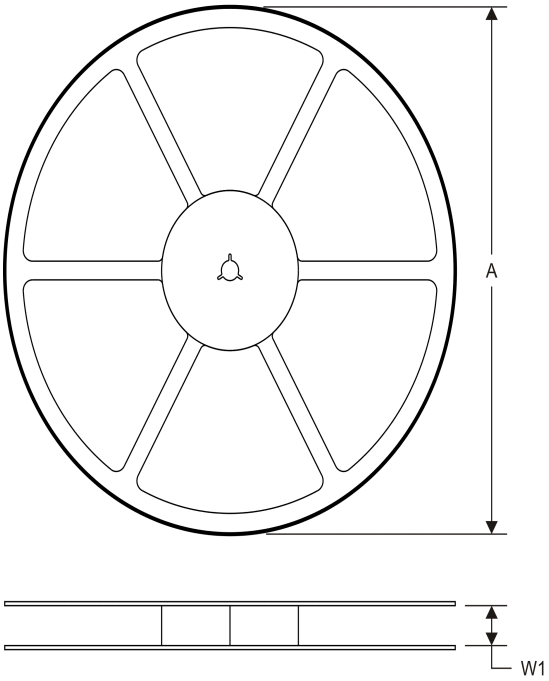
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

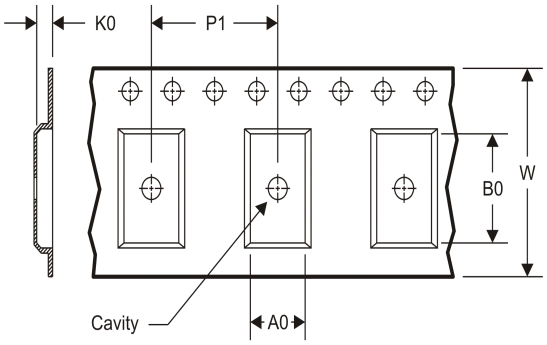
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



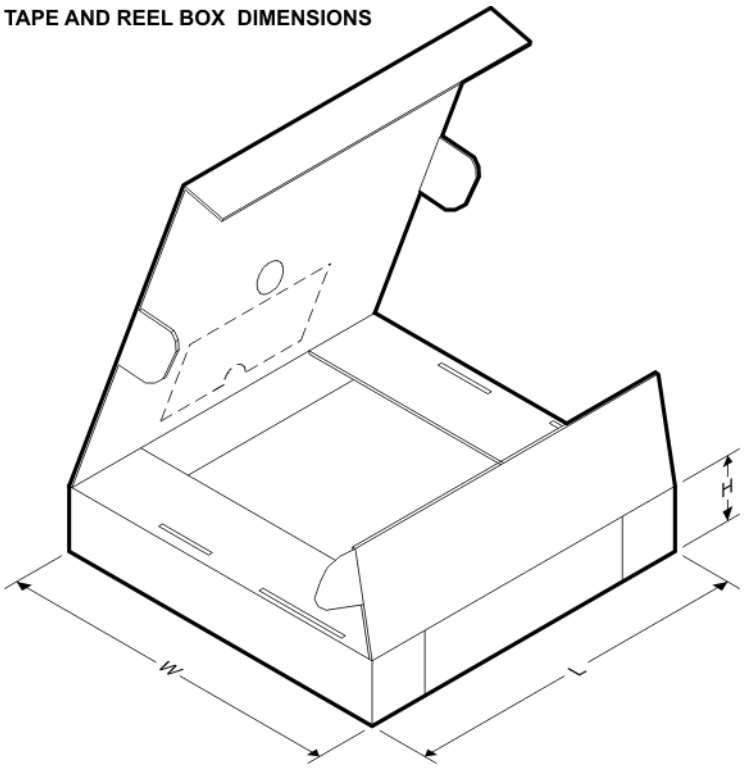
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3116D2DADR	HTSSOP	DAD	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3118D2DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3130D2DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

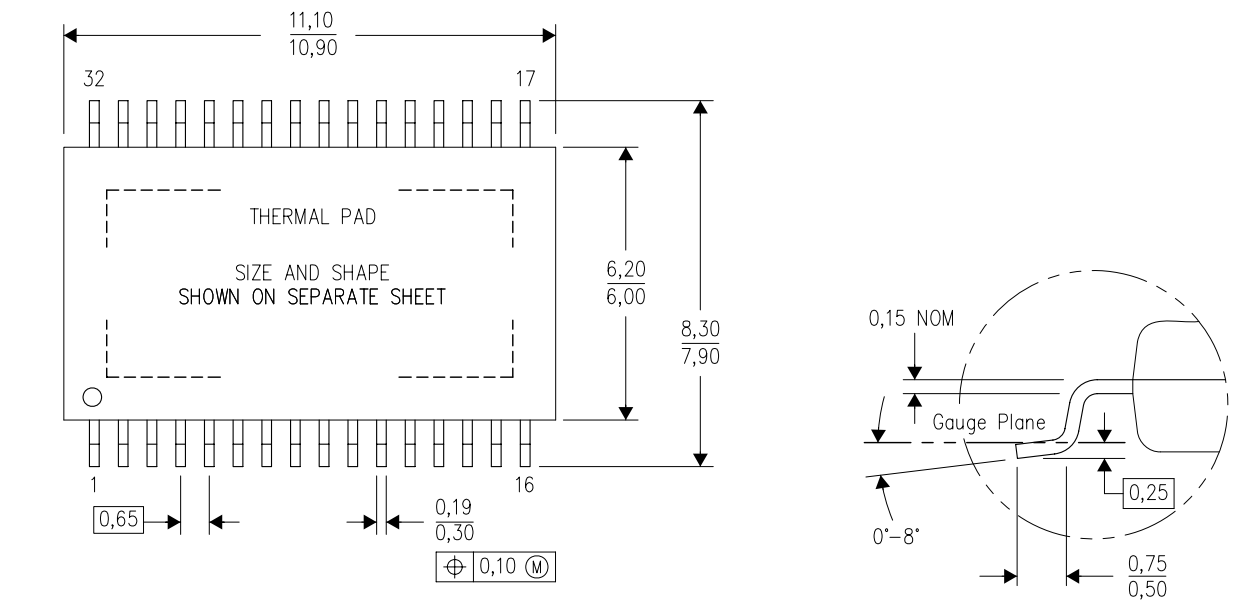
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3116D2DADR	HTSSOP	DAD	32	2000	367.0	367.0	45.0
TPA3118D2DAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0
TPA3130D2DAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073257–4/E 10/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

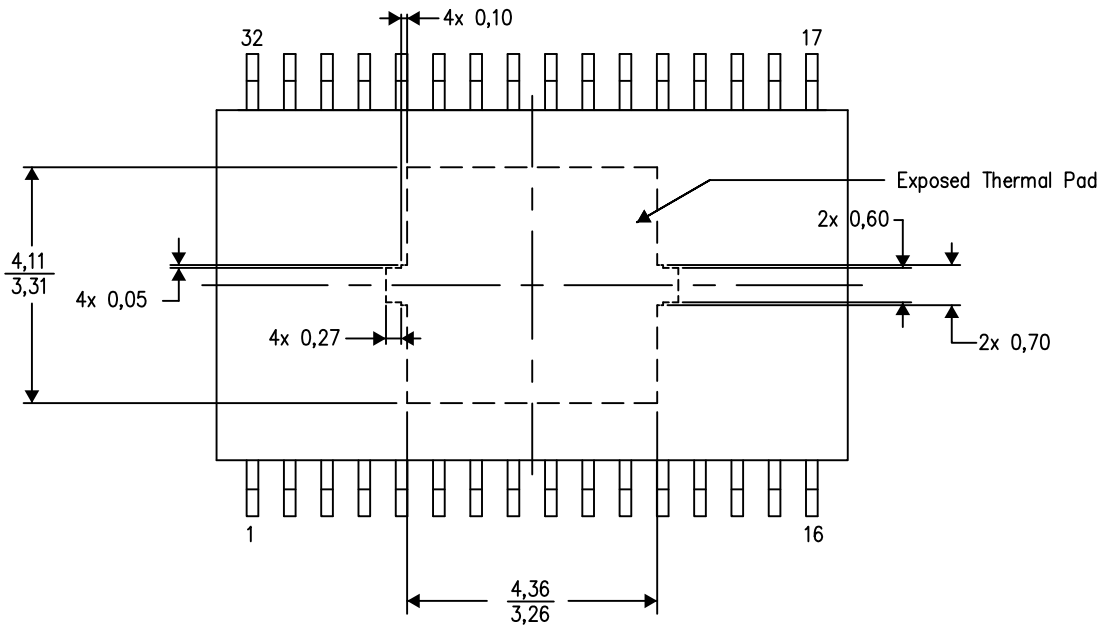
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

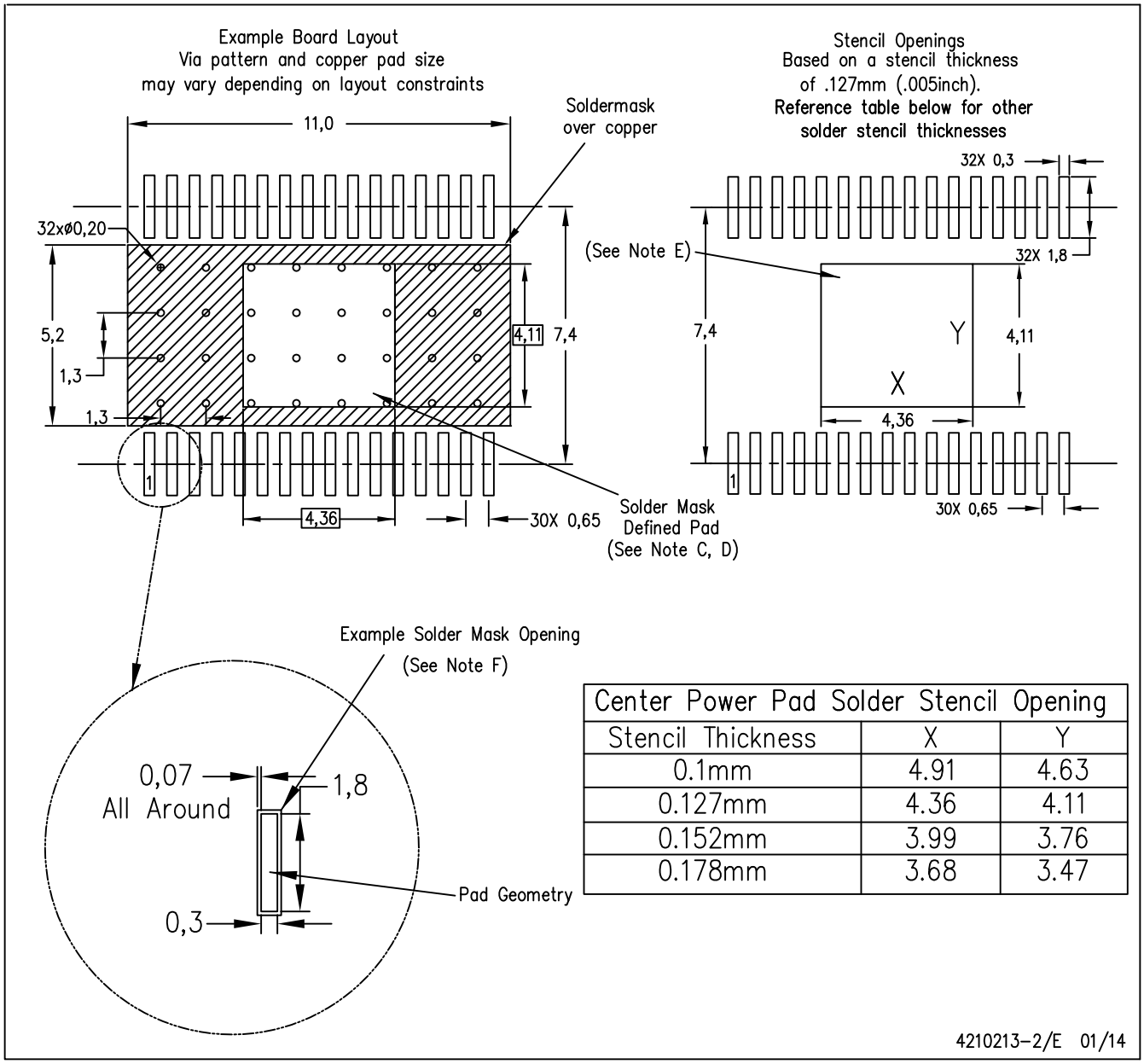
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



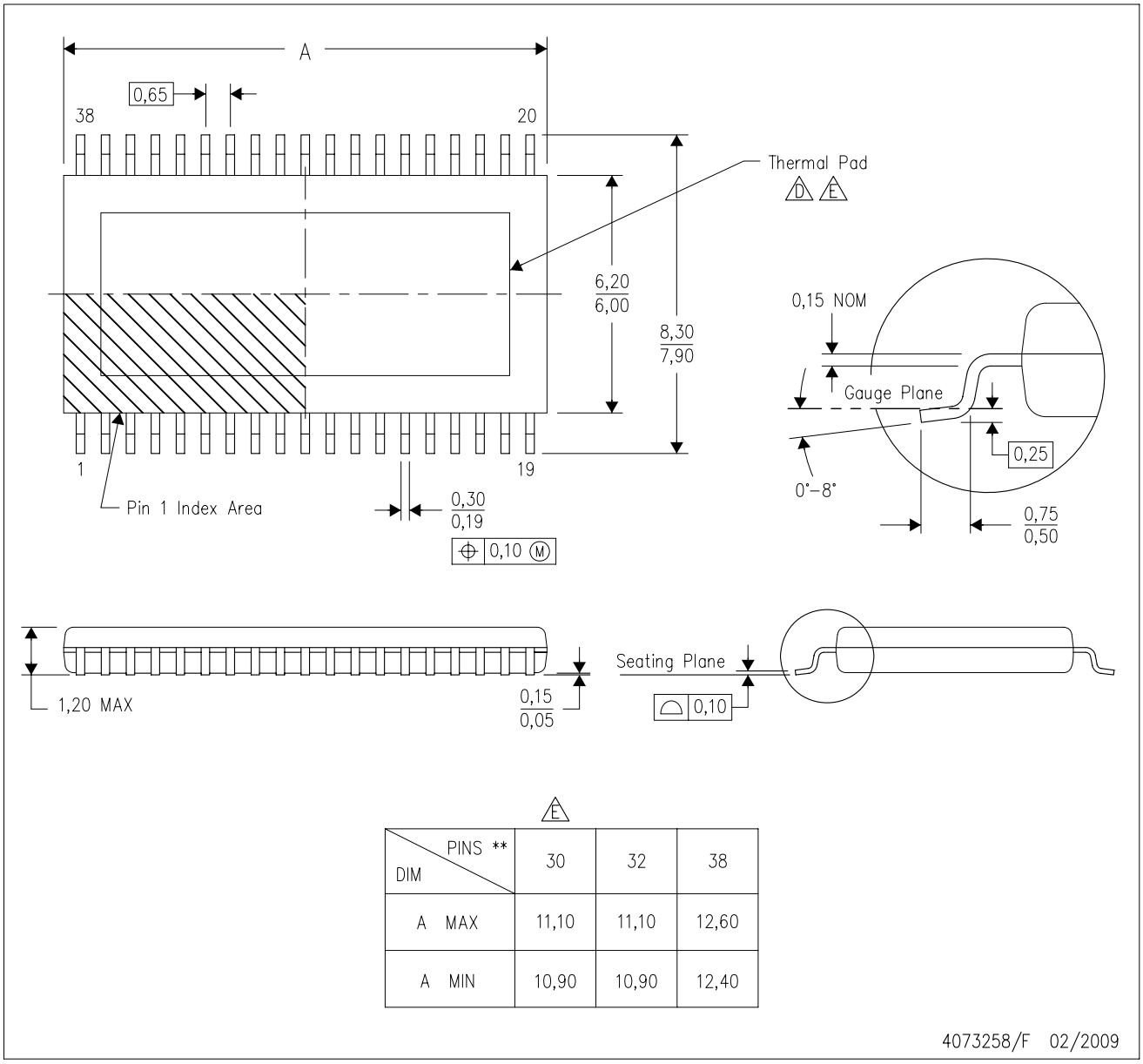
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

4210213–2/E 01/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

DAD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE (DIE DOWN)

38 PIN SHOWN



E

DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4073258/F 02/2009

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153, except 30 pin body length and JEDEC variations for top side thermal pad.

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