Product data sheet

1. General description

The HEF4011B is a quad 2-input NAND gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

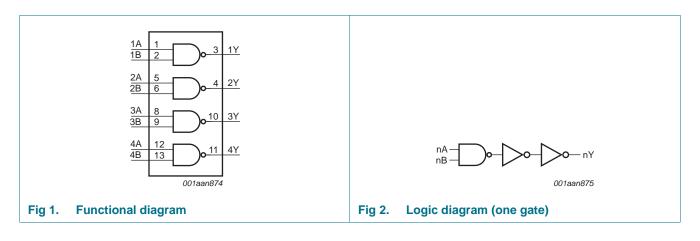
3. Ordering information

Table 1.Ordering information

All types operate from -40 °C to +125 °C

Type number	Package	Package			
	Name	Description	Version		
HEF4011BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1		
HEF4011BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1		

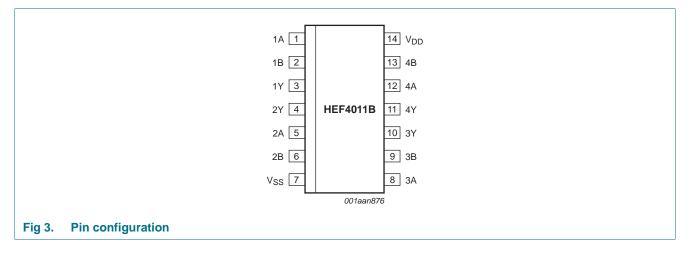
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2.	Pin description	
Symbol	Pin	Description
nA	1, 5, 8, 12	input
nB	2, 6, 9, 13	input
nY	3, 4, 10, 11	output
V _{SS} V _{DD}	7	ground (0 V)
V _{DD}	14	supply voltage

6. Functional description

Table 3.Function table

Input		Output
nA	nB	nY
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

					-
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
l _{IK}	input clamping current	$V_{\rm I} < -0.5$ V or $V_{\rm I}$ > $V_{\rm DD}$ + 0.5 V	-	±10	mA
VI	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_{\rm O}$ < –0.5 V or $V_{\rm O}$ > $V_{\rm DD}$ + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C			
		DIP14	<u>[1]</u> _	750	mW
		SO14	[2] _	500	mW
Р	power dissipation	per output	-	100	mW

[1] For DIP14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 12 mW/K.

[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5 V$	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

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9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_l = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	−40 °C	T _{amb} =	$T_{amb} = -40 \ ^{\circ}C \ T_{amb} = +25 \ ^{\circ}C \ ^{\circ}$		T _{amb} = +85 °C		T _{amb} = +125 °C	Unit	
				Min	Max	Min	Мах	Min	Max	Min	Max		
VIH	HIGH-level	$ I_0 < 1 \ \mu A$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V	
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V	
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V	
V _{IL}	LOW-level	$ I_0 < 1 \ \mu A$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V	
	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V	
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V	
V _{OH}	HIGH-level	$ I_0 < 1 \ \mu A$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V	
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V	
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V	
V _{OL}			$ I_0 < 1 \ \mu A$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
I _{OH}	HIGH-level	$V_{O} = 2.5 V$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA	
	output current	V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mΑ	
		$V_{O} = 9.5 V$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA	
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA	
l _{OL}	LOW-level	$V_O = 0.4 V$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA	
	output current	$V_O = 0.5 V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA	
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA	
I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA	
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ	
		combinations;	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μΑ	
		I _O = 0 A	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ	
Cı	input capacitance			-	-	-	7.5	-	-	-	-	pF	

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $T_{amb} = 25$ °C; for waveforms see <u>Figure 4</u>; for test circuit see <u>Figure 5</u>; unless otherwise specified.

Symbol	Parameter	Extrapolation formula ^[1]	V _{DD}	Min	Тур	Max	Unit
t _{pd}	propagation delay	28 + 0.55 × C _L	5 V	[2] _	55	110	ns
-		$14 + 0.23 \times C_L$	10 V	-	25	45	ns
		$12 + 0.16 \times C_L$	15 V	-	20	35	ns
t _{THL}	HIGH to LOW output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

Table 8. Dynamic power dissipation

 $V_{SS} = 0 V; t_r = t_f \le 20 ns; T_{amb} = 25 \ ^{\circ}C.$

Symbol	Parameter	V_{DD}	Typical formula	Where
PD	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_DD^2 \ (\muW)$	f_i = input frequency in MHz;
		10 V	$P_D = 6000 \times f_i + \Sigma(f_o \times C_L) \times V_DD^2 \text{ (}\muW\text{)}$	$f_o = output frequency in MHz;$
		15 V	$P_{D} = 20100 \times f_{i} + \Sigma(f_{o} \times C_{L}) \times V_{DD}^2 \; (\muW)$	C_L = output load capacitance in pF;
				$\Sigma(f_o \times C_L)$ = sum of the outputs;
				V_{DD} = supply voltage in V.

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11. Waveforms

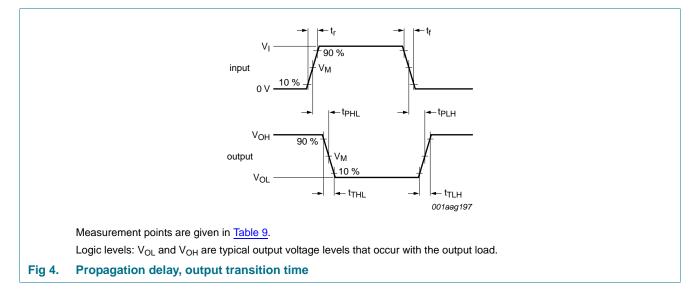


Table 9. **Measurement points**

Supply voltage	Input	Output
V _{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}

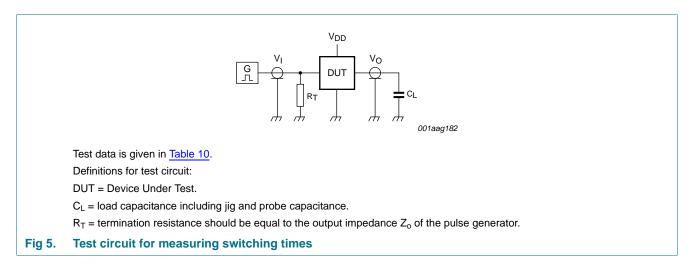


Table 10. Test data

Supply voltage	Input		Load
V _{DD}	VI	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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12. Package outline

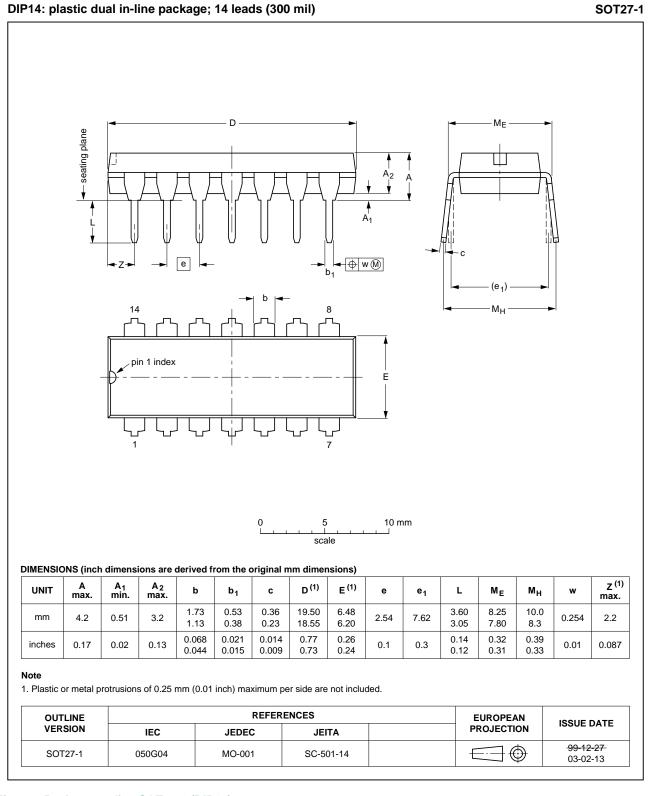
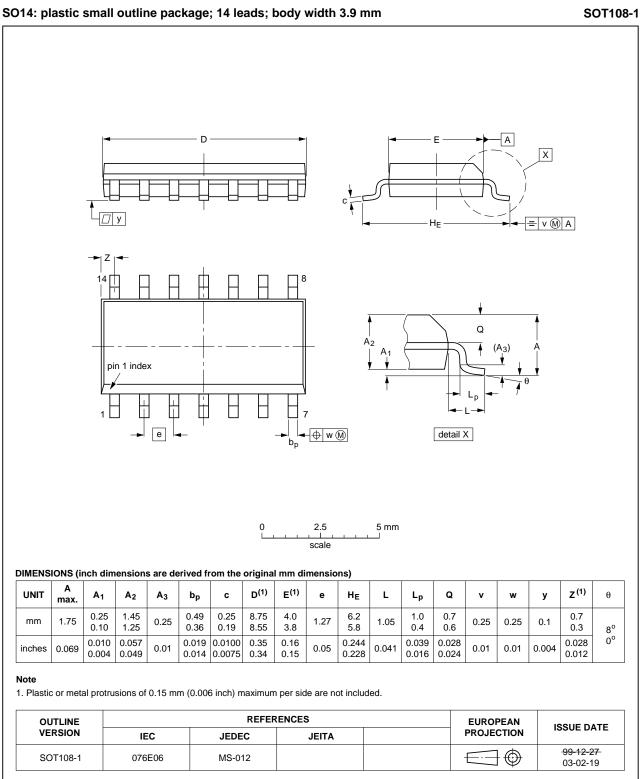


Fig 6. Package outline SOT27-1 (DIP14)

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Package outline SOT108-1 (SO14) Fig 7.

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13. Abbreviations

Table 11.	1. Abbreviations	
Acronym	Description	
DUT	Device Under Test	

14. Revision history

Table 12. Revision hi	story					
Document ID	Release date	Data sheet status	Change notice	Supersedes		
HEF4011B v.5	20111121	Product data sheet	-	HEF4011B v.4		
Modifications: • Legal pages updated. • Changes in "General description" and "Features and benefits". • Section "Applications" removed.						
HEF4011B v.4	20110330	Product data sheet	-	HEF4011B_CNV v.3		
HEF4011B_CNV v.3	19950101	Product specification	-	HEF4011B_CNV v.2		
HEF4011B_CNV v.2	19950101	Product specification	-	-		

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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